Processor Design Verification Using the Hybrid Emulator

YAMADA Kazuo, NISHIMOTO Hiroaki, DAITO Masayuki, ONO Hirohiko

Abstract

Techniques for executing system verification using an FPGA-based prototyping board are being applied widely before the actual chip fabrication process is completed. For the verification of the next-generation processors to succeed the V850E1 series, NEC Electronics has recently started the in-circuit emulator (IE) verification at a few months before completion of actual chip fabrication by applying the Hybrid Emulator, a prototype board developed at NEC's System IP Core Research Laboratories. In addition, NEC Electronics has also constructed an environment for system verification and SW benchmarking using the custom debugging function mounted in the Hybrid Emulator. This enables promotional activities based on customer benchmark measurements and the evaluation of compiler improvements resulting in the advancement of the evaluation process timings. This paper is intended to introduce the application of the hybrid emulator in processor verifications.

Keywords

emulator, co-verification, processor development, evaluation process, in-circuit emulation advance verification, performance evaluation, development tool, custom debugger

1. Introduction

Of importance in the development of processor LSIs is not only a reduction of the LSI development period but also a reduction in the period of preparation of development environments including that of the in-circuit emulator (IE), the compiler and the OS.

In the recent development of the next-generation processors to succeed the current V850E1, we introduced an FPGA-based prototyping board developed by NEC's System IP Core Research Lab, called the Hybrid Emulator. This is a pioneering advance in the microcomputer evaluation process that is aimed at shortening the design period by advancing the timing of the IE verification process.

2. The Microcomputer Evaluation Process and the Purpose of the Introduction of Hybrid Emulator

Fig. 1 shows the evaluation process of a microcomputer. After the register transfer level (RTL) circuit verification, the microcomputer and the evaluation board are fabricated and the in-circuit emulator (IE) is developed using a sample chip.

The IE accesses the debug control unit (DCU) in the CPU using the boundary scan function of the JTAG serial communication standard and provides functions including program execution, breaking and monitoring on the CPU.

Since the control and debugging of the actual chip are executed using the IE function, it is required to begin evaluation with the IE operation check and then proceed to the HW verification and the SW benchmarking.

As the IE and CPU debugging protocols of the next-generation processor are compliant with the NEXUS standard protocol which is different from the one adopted for the previous processors, they were also subjected to our verification process.

One of the purposes of the introduction of the FPGA-based

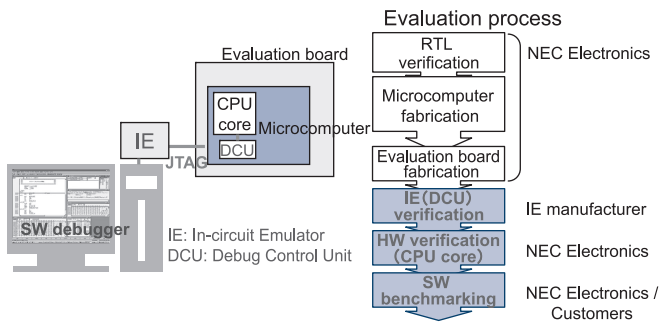


Fig. 1 Traditional microcomputer evaluation process.

prototyping board was to advance the timing of the IE verification before completion of the actual chip fabrication by mapping its circuitry on the FPGA instead of as for the previous evaluation method with which the IE evaluation was executed by starting up the IE board after completion of the actual chip fabrication.

Another purpose was to check the system operation by executing the SW verification and processor performance benchmarking as early as possible using the custom debugger function of the Hybrid Emulator, without using the IE interface.

3. Hybrid Emulator Function

3.1 Outline

On the PC the Hybrid Emulator consists of the Hybrid Board mounting the FPGA and the SW simulator (ClassMate) as shown in **Fig. 2** .

The debugging functions of the Hybrid Board mounting the FPGA and the SW simulator on the PC are coordinated by means of the clock transmission and data communication management mechanism.

The characteristic advantage of the Hybrid Emulator that is not found with ordinary FPGA-based prototyping boards is that it has the components (libraries) featuring Features 1 and 2 (described later). This feature provides the flexibility for constructing a debugging environment covering circuit control and monitoring in a short period by combining the components according to the circuit structure. The debugging function is a basic one compared to that of the dedicated debug control unit (DCU) mounted in the processor. It offers an advantage unavailable with the previous IE-based verification environment, which is the possibility of customizing the observations of characteristics not covered by the DCU.

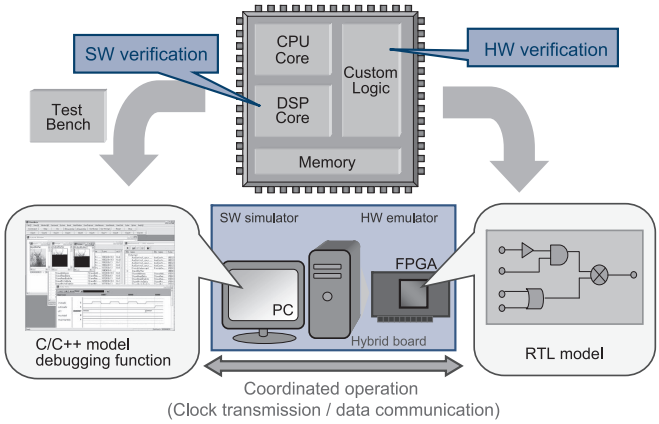


Fig. 2 Hybrid Emulator.

3.2 Feature 1: HW Control Basic Block Library

To enable the break condition setting and execution control of the HW while emulating it at a high speed using the clock on the board, the following library of basic blocks is provided (**Fig. 3**).

(1) Clock Control Block

This block controls the clock generation including the dividing clock.

(2) Break Control Block

This block sets and manages the break conditions for temporary breaks in execution.

(3) Program Counter (PC) Control Block

When the CPU is mounted on the FPGA, this block manages the verification SW execution using the SW debugger.

These basic control blocks have interfaces for enabling the setting from the custom debug library described in Feature 2 in the following section, 3.3, and control the execution of the circuit based on linkage with the break setting on the SW debugger. This allows the PC to debug the SW and to evaluate its performance during high-speed execution in the MHz order on the FPGA.

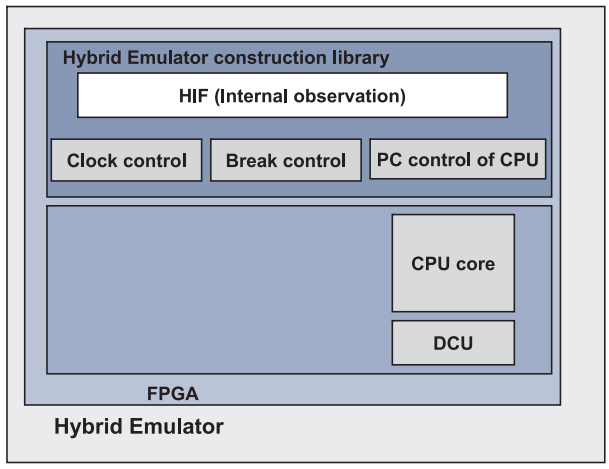


Fig. 3 Hybrid Emulator construction library.

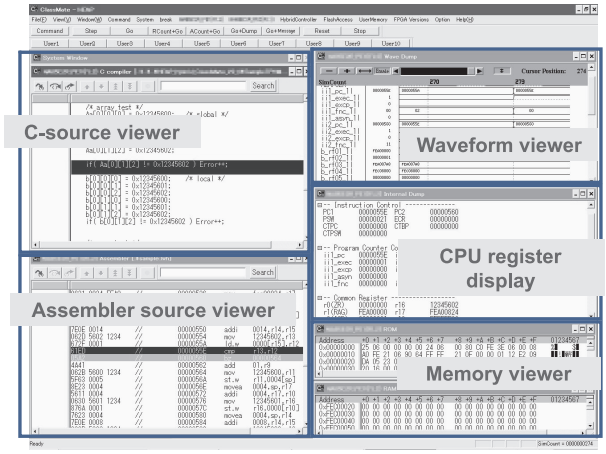


Fig. 4 Debug viewers provided by ClassMate.

3.3 Feature 2: Custom Debug Library

The Hybrid Emulator utilizes the GUI-based custom debug library provided by our cycle-based SW simulator "ClassMate" (**Fig. 4**)

(1) C-Source Viewer and Assembler Source Viewer

These viewers provide the source line debug function for the C-source and assembler for use in SW debugging. It also allows the break setting and step execution based on the GUI source line.

(2) Waveform Viewer, CPU Register Display and Memory Viewer

The HW signal waveform viewer and memory viewer provide the debugging functions required for HW/SW verifications. The HW registers can be set from the custom debugger so that prototype verification of the altered HW configuration is possible without remounting to the FPGA architecture.

4. Protocol Verification Using IE (IE Verification)

For the protocol verification using IE, which is our primary purpose, we used mainly the functions of the FPGA board of the Hybrid Emulator, and built an environment connected to the IE through a connection board as shown in **Fig. 5** .

The verifications consisted of checking of the CPU-dependent functions including the normal communication based on the NEXUS standard protocol, the CPU execution control from the IR, and tracing and monitoring.

The internal signals of the DCU communicate with the IE.

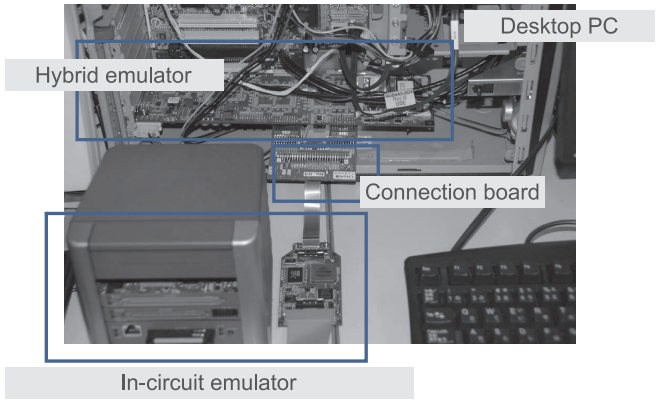


Fig. 5 Protocol verification using in-circuit emulator.

By extracting these signals to the debug viewers of ClassMate, we enabled IE verifications while observing the DCU's internal signals, which is a difficult process on the fabricated actual chip. With regard to the difficulty in obtaining the expected operations with the connection to a completed IE environment, we succeeded in pinpointing and solving the problems by using this function.

As a result of the early construction of the IE environment and advancement of the verification timing, we were able to discover a problem in the RTL before the silicon fabrication and thereby avoid respinning.

5. SW Development Resources and Processor Performance Benchmarks

The development of the IE verification environment including the connection board occupied us for several months but concurrently with this work, we were able to construct the custom debug environment of the Hybrid Emulator (Hybrid debugging system), which was the second aim of our program.

In the construction of the environment, we combined a basic HW control library and custom debug library in accordance with the hardware structure of the next-generation processor. We also improved the SW debugger display and extracted the required monitor signals according to their characteristics. The preparation of a basic library has made it possible to start the SW development environment for the assembler and compiler before the start of IE verifications, also enabling early measurement of the performance of the new CPU. This environment served us for the advance checking of the anticipated functions and performance.

The introduction of this environment enabled SW performance benchmarking by prospective microcomputer users at an early stage and before the sample shipment. The SW calculation accuracy (number of execution cycles) has recently become a critical factor for the processors for car-mount use. In this regard the capability of SW benchmarking with the same cycle accuracy as the actual chip is expected to make information readily available for use in the microcomputer industry, as well as contributing to improvements in the design quality.

From the viewpoint of microcomputer product planning, the availability of a prototype with the same accuracy as the actual chip fabricated device is useful in enabling highly accurate performance evaluation. In addition, the possibility of confirming detailed specifications and performances with the same accuracy as the actual chip fabricated device also enables the accurate answering of customer inquiries.

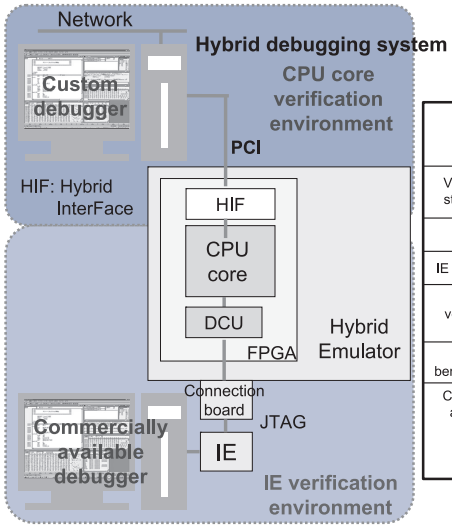
6. Improvements to the Microcomputer Evaluation Process

Application of the Hybrid Emulator in the processor design verification environment enables concurrent execution of IE design, fabrication and verification processes, SW benchmarking and HW/SW co-verification (**Fig. 6**). Consequently, microcomputer verification can now be advanced by a few months compared to the previous situation, as shown in **Fig. 7** .

7. Future Development: Implementation of a Processor Verification Environment Platform

If the processor verification environment is constructed for each product or purpose, a timely deployment of products is difficult because of the need for specified startup times.

In order to avoid the above and improve the efficiency of the startup of the verification environment, we are planning to implement the processor + peripheral macro verification environment into a platform. Because the Hybrid Emulator incorporates several FPGAs it can improve the efficiency of the verification environment startup work by mounting the CPU core in a specific FPGA in advance in order to turn it into a verification platform while mounting the circuits of individual products in non-used FPGAs. This strategy is expected to improve both the verification quality and the efficiency of the verification environment architecture.



	Hybrid debugging	Hybrid + IE verification	(Reference) Traditional IE verification
Verification start timing	After RTL verification	After RTL verification	After on-chip implementation
DCU	Unnecessary	Necessary	Necessary
IE verification	×	◎	◎
HW verification	◎ (HW internal observation)	○	○
SW benchmarking	◎	○ (After IE verification)	○ (After IE verification)
Clock cycle accuracy	◎ (Same cycle as on-chip)	○ (Time measurement using program/timer)	○ (Time measurement using program/timer)

◎: Suitable. ○: Possible. ×: Unsuitable

Fig. 6 Processor design verification environment the using Hybrid Emulator.

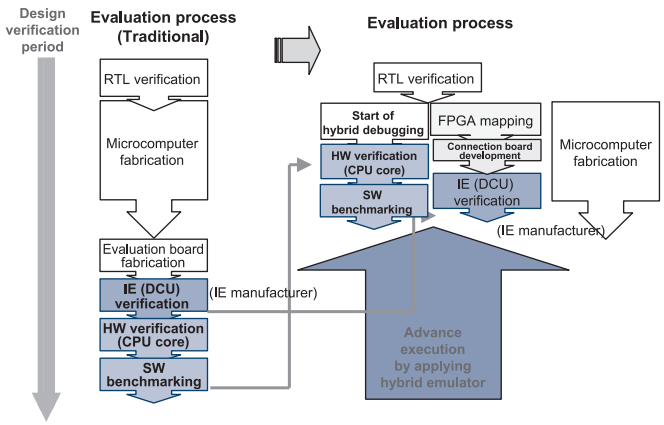


Fig. 7 Advance execution of the microcomputer evaluation process.

8. Conclusion

We confirmed the effect of shortening the design/verification period in the introduction of the Hybrid Emulator for processor design verifications. In the future, we will expand the application of this technology outside the domain of processor design verification. The new architecture will cover processor performance evaluation at an equivalent level to the evaluation of the system-on-chip. Processor product planning, advance confirmation of processor specifications and preparation of peripheral environments including for the processor as well as for development environments will also be dealt with.

Reference

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Authors' Profiles

YAMADA Kazuo
Manager,
Design Engineering Development Division,
Technology Foundation Development Operations Unit,
NEC Electronics Corporation

NISHIMOTO Hiroaki
Assistant Manager,
2nd System-on-a-Chip Design Division,
NEC Micro Systems, Ltd.

DAITO Masayuki
Department Manager,
1st Microcomputer Division,
Microcomputer Operations Unit,
NEC Electronics Corporation

ONO Hirohiko
Group Manager,
Microcomputer Software Division,
Microcomputer Operations Unit,
NEC Electronics Corporation