Present Status of the Embedded CPU in SoC Design

SAKURAI Yoshikazu, SUZUKI Hiroaki, MAEMURA Kouji, TAKAKURA Satoshi

Abstract

Most current System on Chip (SoC) devices incorporate embedded CPUs that have an important function.

The SoC design is complicated and its functions are advancing every year. The times in which only the individual performance of an embedded CPU was in question has now changed to one in which emphasis is put on the bus configuration design in accordance with the requirements of each application and on the design of distributed data processing.

This paper is intended to describe the present status of the embedded CPUs that are provided by NEC Electronics for the "customer-intimate ASIC" developed by the user and semiconductor vendor for each application such as a digital home appliance or cellular phone. It also introduces the core and platform based design solutions of the British company ARM Limited.

Keywords

System on Chip (SoC)

1. Requirements for Embedded CPUs

The embedded CPU of SoC devices has traditionally been at the center of system control, playing the role of running single data flow on a simple basis, so that the system performance has been dependent on the CPU performance. In the current SoC devices, the range of applications of the CPU has been so expanded that the embedded CPU is required to determine the optimum solution for each application. It must feature a high processing and transfer capability for operations such as video compression and expansion, by accurately estimating the overall system bus structure and the frequency transfer band of each of its sections. For this purpose, a technique is often used to build the CPU architecture and bus configuration independently and distribute data processing that would impose a heavy load on a single CPU to multiple processors, DSPs and exclusive hardware. As a result of such a solution, the requirements for embedded CPUs are now focused on flexibility and scalability in system construction as well as on processing performance. Based on such a background, CPU cores such as the ARM core of the British company ARM Limited and the MIPS core of the American company MIPS Technologies have come to occupy a large share in the embedded CPU sector as *de facto* standards.

2. Lineup of Embedded CPUs at NEC Electronics

At NEC Electronics, we have developed a range of CPUs for ASICs based on the ARM Limited core range.

We have acquired the licenses for the CPUs from the low end models (ARM7 Family) to the middle-end (ARM9 Family) and high end models (ARM11 Family) and provide them together with the V850E core, which is NEC Electronics' original CPU, as shown in the roadmap of the CPUs we are currently offering in **Fig. 1**. We also offer the ETM (Embedded Trace Macrocell) for improving debugging efficiency and the VFP (Vector Floating-Point Processor) as the associated IPs and a secondary linked cache controller. For the ASICs, our lineup is centered on the CB12 (0.15µm,) which is also compatible with the CB130 (0.13µm) and CB90 (90nm) processors as well as with the most advanced processors that are being developed for the future.

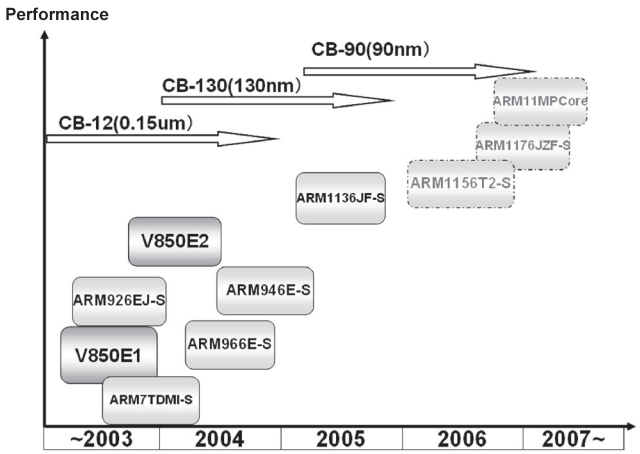


Fig. 1 CPU roadmap.

3. SoC Design Mounting ARM Cores

In general, the architectures of the ARM core devices provided as IPs are prohibited from being modified by the manufacturers. Therefore, it is possible to obtain high software compatibility (covering the debugging function) and high design quality with the devices of any vendor and high design quality, which enables flexibility for the vendors of ARM.

However, their implementation varies depending on the design method and process adopted. Specifically, it is possible to modify the configurations according to the system parameters such as the internal cache size, TCM (Tightly Coupled Memory) size, the use of ETM and the use of VFP. In addition, it is also possible to select physical targets such as the core area, operation speed and power consumption. At NEC Electronics, we implement the CPUs as hardware macros by providing them with these variations in advance. The hard macro system can hasten the timing convergence in ASIC design and facilitates an increase in speed, reduction of area and reduction of power consumption that are hard to achieve with the software macro. The IPs with hardware macros are provided for the user as libraries (STA library, layout library, etc.). If there are individual requests (short TAT, special process, etc.) for an IP, it is also possible to select the soft macro development flow. With both the hardware macro and software macro systems, the user can design the SoC without considering the information and timings inside the IP.

What is most characteristic with the SoC design using ARM core devices is that the logical simulations are performed using the simulation model called DSM (Design Simulation Model) instead of the net list (by considering the protection of the IP). The DSM is capable of efficient system verification because it is a cycle accurate model and that it can output powerful debugging information on the observation of internal registers and the tracing of instructions and data executions.

We have added some functions to the DSM so that it can identify troubles in the gate simulation by checking the bus protocols, annotating timings to achieve the same accuracy as the STA and checking timings.

Furthermore, for the trace output for which it is usually difficult to confirm the operation and the debugging functions such as the JTAG interface, we provide system verification kits and abundant documents to facilitate design and verification by the users.

4. SoC Development Styles

The design and development styles of SoC are not uniform depending on the requirements for the application fields, development costs, TAT, etc. From the viewpoint of the allotment of development, the SoC products can be classified into the ASSPs (Application-Specific Standard Products) with which a chip vendor performs consistent operations from specifications to design and provides the product as standard and the ASCPs (Application-Specific Custom Products) with which the users determine the specifications and design. The ASCPs are generally called ASICs (Application-Specific Integrated Circuits).

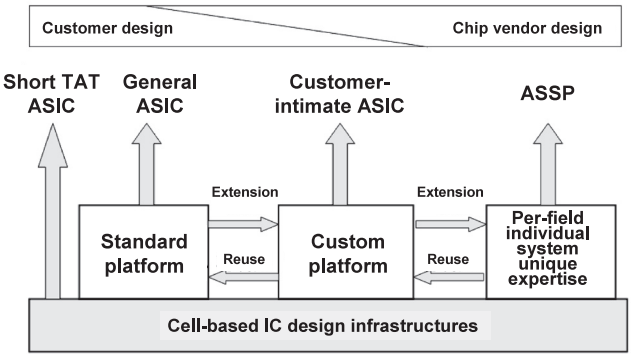


Fig. 2 SoC development styles.

Among the ASICs, those with which the system is built based on development operations by both the user and chip vendor are called the customer-intimate ASICs (**Fig. 2**). This type is seen with digital home appliances such as printers and digital cameras as well as with large-scale systems for advanced applications such as cellular phone systems.

What is important in this development approach is the definition of interfacing between the user and chip vendor (logical/physical specifications, design allotment, quality check, etc.). In order to clarify it, it is required to provide a standardized design environment and an IP base design environment using an IP implemented as a library, while the user is required to provide the scalability and flexibility for a design environment specialized for the field in question as well as a verified system. This is made possible by the platform base design described in the next section.

5. Provision of a Platform Based Design

From the viewpoint of SoC design, the construction of subsystems and bus configurations incorporating embedded CPUs is still a complex subject for many users and presents a bottleneck in the design and verification TAT. In addition, standardization of CPUs has made it easier to reuse designs and close relationships between IP vendors and chip vendors have resulted in embedded CPU

expertise being accumulated by the chip vendors. Thus, the design foundations involving the embedded CPU and CPU subsystems are now regarded as matters to be prepared by the chip vendors.

With customer-intimate ASICs, particularly in their bus configurations, the bus masters have increased according to the need for distributed data processing and the configuration of the buses between IPs are changing from the common bus to more complicated configurations such as the multilayer bus, hierarchical bus and crossbar switch. In addition, each IP is provided with an RTL and test bench assuming that it is used separately, but the users are in fact occupied with the connection of IPs, construction of IP subsystems and confirmation of mutual operations.

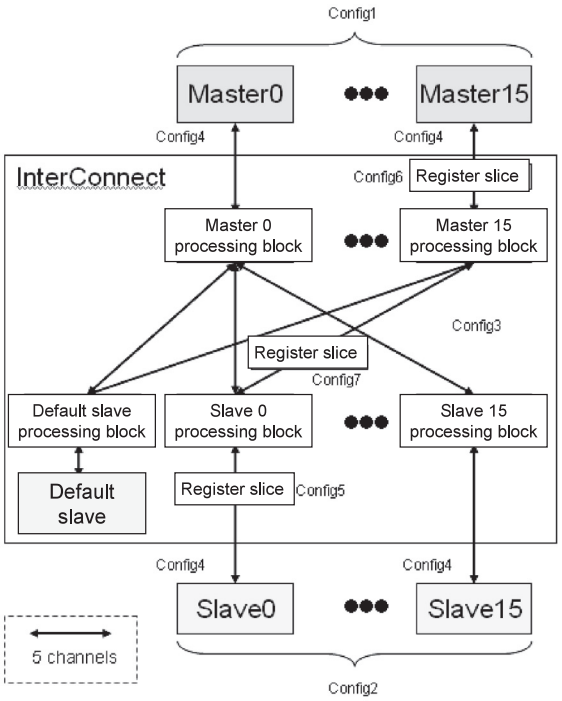
At NEC Electronics, we prepare systems in which IPs are connected using the standard bus in advance and provide them for users after completing the previous quality check. We have also prepared the standard buses as IPs (BUSIPs) and constructed an environment that generates the RTL required for bus configuration automatically according to the selection of the system parameters. These include: the bus width, address map, number of masters, number of slaves, number of register slices in bus and the number of layers.

This procedure enables users to build subsystems and to determine tradeoffs with respect to the requirements of the application at an early stage. **Fig. 3** shows the variable parameters of the AXI bus and an example of system configuration.

Timely system construction leads to an early completion of system performance checks using FPGA and to the parallel development of software. For the quality, too, early quality improvement is achieved by facilitating the introduction of assembly/verification tools by assuming the use of the standard bus. Also, the additional introduction of IPs from outside companies will be facilitated thanks to the clarity of the interfaces.

A platform per user and per application field that is built using such a technique will be easy to be diverted or extended to other platforms in the future. We believe that it allows users to concentrate resources on the essential sections related to their own applications and thereby to differentiate themselves from competitors with added values.

At present, NEC Electronics are capable of undertaking CPU subsystem development based on summarized specifications received from the user and provide CPU subsystems in short TAT. This can reduce the TAT and costs required for building the optimum ASIC for each system requirement. In addition, we have also



Config. No.	Item	Setting Range
Config. 1	Number of masters	1 to16
Config. 2	Number of slaves	1 to16
Config. 3	Connection destination	Specified/Not specified Example) M15 to S15 Not specified
Config. 4	Data width	32, 54, 128
Config. 5	Slave I/F register slice	0, 1 Example) S1 1
Config. 6	Master I/V register slice	0, 1 Example) M1 1
Config. 7	Master-slave register slice	0, 1 Example) M15 to S0 1

* Setting items of each master
- ID width
- Number of issued read transactions
- Number of issued write transactions

Setting items of each slave
- Number of received read transactions
- Number of received write transactions
- Write interleave depth
- Number of areas
- Address range

Fig. 3 Variable parameters of the AXI bus, example of system configuration.

prepared line ups of AMBA basic IPs (memory controllers, DMA controllers, etc.), peripheral IPs (timers, serial and universal ports, etc.) as well as the platform based design infrastructures such as the evaluation CPU chips, evaluation board simulation models, test benches and documents. NEC Electronics have named this infrastructure system the MICROSSP.

The MICROSSP presently includes subsystems centered on ARM cores and the V850E Core (**Fig. 4**).

We can also offer an evaluation board on which the V850E1/V850E2/ARM946E-S/ARM926EJ-S test chips can be mounted (**Photo**).

At NEC Electronics, the number of staff engaged in the ARM subsystem design is increasing rapidly. With the large number of achievements of the ARM core-mounted products, we are accumulating expertise that enables us to build larger scale and more complex systems. These infrastructures make us ready to provide the users with services covering all of the SoC development phases from project assessment to system examination and mass-production.

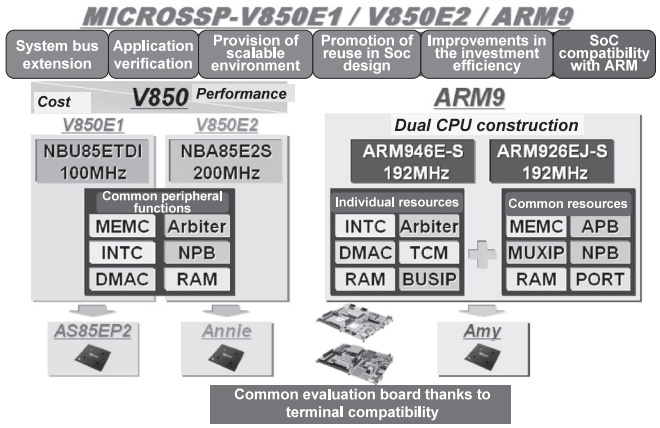


Fig. 4 Concept of MICROSSP.

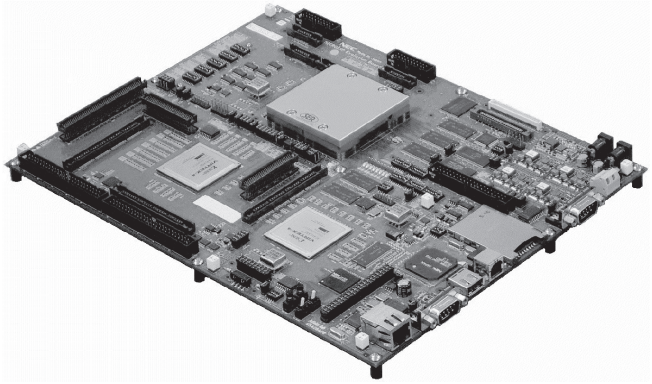


Photo Evaluation board.

6. Conclusion

In the above, we have introduced details of our efforts with regard to the embedded CPU and platform based design supporting the SoC design strategy.

NEC Electronics intend to expand the lineup of our embedded CPU products. We will focus particularly on the application of our multicore technology to a wide range of ASICs such as the ARM11 MPCore that we have jointly developed with ARM Limited.

In addition, we will also develop hardware platforms with higher added values by extending their compatibility with the AXI bus system, which is expected to become one of the main bus systems of the next generation.

Authors' Profiles

SAKURAI Yoshikazu
Project Manager,
Full Custom ASIC Division,
1st Systems Operations Unit,
NEC Electronics Corporation

SUZUKI Hiroaki
Senior Design Engineer,
Full Custom ASIC Division,
1st Systems Operations Unit,
NEC Electronics Corporation

MAEMURA Kouji
Department Manager,
2nd System-on-a-Chip Design Division,
NEC Micro Systems, Ltd.

TAKAKURA Satoshi
Project Manager,
2nd System-on-a-Chip Design Division,
NEC Micro Systems, Ltd.